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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,707	01/24/2002	Teruhiko Kamigata	1614.1210	7916

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EXAMINER	
INGBERG, TODD D	
ART UNIT	**PAPER NUMBER**
2193	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,707	KAMIGATA ET AL.	
	Examiner	Art Unit	
	Todd Ingberg	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 13 have been examined.

Before Amendment entered.

Drawings

1. Replacement drawing sheets received on June 1, 2005 require a correction. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the term "Conventional System" should be replaced with the label "PRIOR ART". The convention was known at the time of filing. It is prior art the label must be corrected. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

2. Amendment to the Specification filed June 1, 205 has been entered.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Rejection to claims 1 – 12 under 35 U.S.C. 101 has been overcome by amendment.

For new claim 13

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim13 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention is not tangible. The claimed invention is deemed an abstract idea.

Claim 13
A method for aiding instruction processing, comprising: arranging variable-length instructions to be executed in an order; and verifying an arrangement of the variable-length instructions.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN # 5,640,588 **Vegesna** published June 17, 1997 in view of Admitted Prior Art as Disclosed in the Background of Invention Section of the Specification.

Claim 1
Vegesna teaches a method for instruction processing executing on a computer, comprising: identifying a classification of a functional unit which can execute a basic instruction(Vegesna, Abstract, Each of the instructions is classified....); determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot(Vegesna, Abstract, the classifications include memory reference, operations, integer operations ...) : and assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot. It is APA who teaches logical instruction slot (APA, Figure 5) ; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot (APA, figure 5). Although, Vegesna teaches classifying instructions and loading instructions. Vegesna does not explicitly teach a and said logical instruction slot ; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot. It is APA who teaches logical instruction slot (APA, Figure 5) ; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot (APA, figure 5). Therefore, it would have been obvious to one of

ordinary skill in the art at the time of invention to combine the teachings of Vegesna and APA, because optimization of VLIW instructions make programs run faster.

Claim 2
The method for instruction processing as claimed in claim 1, wherein said identifying is divided into identifying an instruction category of a basic instruction (Vegesna, Abstract, classification) , and identifying a classification of a functional unit which can execute said instruction category(Vegesna, Abstract, classification).

Claim 3
The method for instruction processing as claimed in claim 1, further comprising, prior to said checking a relationship between said basic instruction that can be assigned to said logical instruction slot (Figure 6) and other basic instructions to be assigned to other logical instruction slots (APA, Figure 5) .

Claim 4
The method for instruction processing as claimed in claim 2, further comprising, prior to said assigning, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots. As per claim 3.

Claim 5
The method for instruction processing as claimed in claim 3, wherein said determining includes a step of identifying said logical instruction slot having a lowest numeral determined to be assignable. (Interpreted to be FIFO – inherent for deterministic results).

Claim 6
The method for instruction processing as claimed in claim 4, wherein said assigning includes identifying said logical instruction slot having a lowest numeral determined to be assignable. As per claim 5.

Claim 7
The method for instruction processing as claimed in claim 3, wherein said identifying, determining, checking and assigning are repeated for all instruction slots. .(APA, Figure 6)

Claim 8
The method for instruction processing as claimed in claim 4, wherein said identifying, determining, checking and assigning are repeated for all instruction slots. As per claim 7.

Claim 9
A computer program executing on a computer and stored on a computer readable medium, comprising: a classification of a functional unit which can execute a basic instruction; determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical

instruction slot: and assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot. As per the rejection for claim 1.

Claim 10
A computer program as claimed in claim 9, wherein said identifying is divided into identifying an instruction category of a basic instruction, and identifying a classification of a functional unit which can execute said instruction category. As per the rejection for claim 2.

Claim 11
The computer program as claimed in claim 9, further comprising, prior to said assigning, for checking a relationship between said basic instruction than can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots. As per the rejection for claim 3.

Claim 12
The computer program as claimed in claim 10, further comprising, prior to said assigning, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots. As per the rejection for claim 4.

Claim 13
Vegesna teaches a method for aiding instruction processing (**Vegesna,** Col 8, lines 10 – 15, "in-order"), comprising: arranging variable-length instructions to be executed in an order (**Vegesna,** Col 8, lines 10 – 15, "in-order"); and verifying an arrangement (**Vegesna,** Col 8, lines 15 – 22, " ..next instruction must be...")of the variable-length instructions (APA). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Vegesna and APA, because optimization of VLIW instructions make programs run faster.

Response to Arguments

Applicant's arguments filed June 1, 2005 have been fully considered but they are not persuasive.

The following are the Applicant's remarks. They have been scanned in and may contain some

OCR errors.

Applicant's Remarks

"On page 4 of the Office Action, claims 1-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,640,588 (Vegesna) in view of the conventional systems and methods described in the specification of the present invention (e.g., Figure 5 and accompanying text). The application includes only 12 claims. Thus, Applicants will only address the 12 claims of the application and the additional claim 13 added herein by Applicants.

According to Vegesna, it is directed to an apparatus and method for scheduling a sequence of instructions for achieving multiple executions with a Central Processing Unit (CPU). Each instruction is classified according to an execution resource of the CPU that executes the instruction. See column 3, lines 11-35.

The conventional system described in the specification of the current invention is directed to an algorithm to verify an arrangement of basic fixed-length Very Long Instruction Word (VLIW) instructions. The conventional system includes actual instruction slots that are used to store the basic instructions. See Specification, page 2, lines 36-27 and FIG. 1.

According to the present invention, it is directed to a method to verify an arrangement of basic VLIW instructions for language processing systems used on processors designed by variable length VLIW architecture. The method of the present invention includes determining whether a basic instruction can be assigned to a logical instruction slot. According to the present invention, a logical instruction slot is a virtual instruction slot which corresponds to a particular functional unit and can be used to store variable length VLIWs. See Specification, page 28, lines 6-12.

The Examiner admitted in the Office Action that Vegesna does not teach a logical instruction slot. It follows that Vegesna does not teach or suggest, "determining whether said basic instruction can be assigned to a logical instruction slot." Applicants respectfully submit that unlike the present invention, the conventional method and system described in the application also does not teach or suggest, "determining whether said basic instruction can be assigned to a logical instruction slot . . .." Although the conventional method described in the specification includes storing instructions into instruction slots, the instruction slots in the conventional system are actual registers, not logical instruction slots. As shown in FIG. 3, for example, each register can include a VLIW. Therefore, independent claims 1 and 9 are patentable over the conventional method, as the conventional method does not teach, "determining whether said basic instruction can be assigned to a logical instruction slot."

Examiner's Response

The Applicant has misrepresented the Examiner's actual statements. The exact wording of the rejection is was as follows:

"Although, Vegesna teaches classifying instructions and loading instructions. Vegesna does not explicitly teach a and said logical instruction slot ; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot. It is APA who teaches logical instruction slot (APA, Figure 5) ; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot (APA, figure 5). Therefore, it would have been obvious to combine the teachings of Vegesna and APA, because optimization of VLIW instructions make programs run faster."

The Examiner stated the reference did not ***explicitly*** teach. The limitations which are not explicit are the Applicant's own terms from the Background of Invention which is admitted prior art. That portion of the rejection reads as follows:

" ... and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot. It is APA who teaches logical instruction slot (APA,

Figure 5) ; and a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot (APA, figure 5)."

The actual rejection has not been argued. In view of the broader claims the claimed invention remains rejected under the same grounds.

Applicant's Remarks

"As claims 2-8 and 10-12 depend from independent claims 1 and 9, respectively, these claims are also patentable over Vegesna in view of the conventional system and method described in the specification, as neither Vegesna nor the conventional system and method, taken alone or in combination, teaches or suggests the elements of the present invention.

Applicants respectfully submit that claim 13 is patentable over Vegesna, as Vegesna does not teach or suggest, "arranging variable-length instructions to be executed in an order; and verifying an arrangement of the variable-length instructions." Applicants respectfully request that all rejections be withdrawn."

Examiner's Response

For the same reasons for claim 1 the Application remains rejected.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 571 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Todd Ingberg
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TI